## What is claimed is:

[Claim 1] 1. A method of operating a message bus serving to transfer data between a plurality of modules, said plurality of modules being connected to said message bus, said message bus containing a plurality of signal lines, said method comprising:

receiving an indication on a first signal line indicating that said message bus has been granted to a first module contained in said plurality of modules, said first signal line being contained in said plurality of signal lines and said first module being contained in said plurality of modules; and

sending from said first module to a second module a plurality of packets, wherein said first module transmit each bit of each of said plurality of packets on said first signal line.

[Claim 2] 2. The method of claim 1, further comprising requesting said message bus for said first module on a second signal line also contained in said plurality of signal lines, wherein said sending sends another bit of each of said plurality of packets on said second signal line.

[Claim 3] 3. A method of operating a message bus serving to transfer data between a plurality of modules, said plurality of modules being connected to said message bus, said method comprising:

using a first set of signal lines to send control signals in an arbitration phase in which one or more of said plurality of modules request for ownership of said message bus using said first set of signal lines, said first set of signal lines being comprised in said message bus, wherein said first set of signal lines comprise a request line on which a first module requests said message bus for transmission of data and a grant line on which said first module is indicated that said message bus has been granted; and

using said first set of signal lines to send data bits between said plurality of modules in a data transfer phase in which said first module allocated said message bus transfers data on said message bus using said first set of signal lines,

wherein said using said first set of signal lines to send control signals in said arbitration phase comprises:

determining in said first module whether a BUSY signal line is asserted, wherein said BUSY signal line indicates whether any of said plurality of modules is available on said message bus;

requesting from said first module ownership of said message bus by sending a request on said request line if said BUSY line is not asserted; and

receiving a bus grant signal from an arbitration controller on said grant line, wherein said grant signal indicates allocation of said message bus to said first module.

[Claim 4] 4. The method of claim 3 , further comprising sending an address of a second module from said first module using said first set of signal lines, wherein said data is sent by said first module to said second module in said data transfer phase and wherein said second module is also contained in said plurality of modules.

[Claim 5] 5. The method of claim 3 , wherein said first module includes said address of said second module in a control packet, wherein said control packet indicates a number of data packets to be sent by said first module to said second module.

[Claim 6] 6. The method of claim 5, wherein said using said first set of signal lines as data paths in said second duration comprises:

asserting in said first module said BUSY line to indicate ownership of said message bus;

examining a TRDY line to determine whether said second module is ready to receive said number of packets after sending said address on said message bus; and

sending from said first module said number of data packets on said message bus, wherein some bits of each of said number of data packets is sent on said first set of signal lines.

[Claim 7] 7. The method of claim 6, further comprising:

receiving said control packet in said second module;

determining in said second module that said number of packets are directed to said second module by comparing said first address to a self address of said second module; and

asserting said TRDY line to indicate that said second module is ready to receive said number of packets.

[Claim 8] 8. The method of claim 7, further comprising:

determining in said second module whether an uncorrectable error is present in a first packet, wherein said first packet is comprised in said number of data packets;

asserting an ERR signal in said second module to indicate presence of said uncorrectable error;

transmitting said first packet again from said first module upon said ERR signal being asserted;

receiving said packet again and performing said determining and asserting ERR and STOP signal in said second module if said uncorrectable error is present again; and

terminating transferring in said first module after determining both said ERR and said STOP is asserted.

[Claim 9] 9. The method of claim 8, wherein said message bus contains only 4 control signal lines.

[Claim 10] 10. The method of claim 3 , further comprising:

receiving in an arbitration block said request on said request line;

determining a first priority group in which said first module is assigned, wherein said first priority group is contained in a plurality of priority groups, wherein a second priority group has a higher priority than said first priority group;

allocating said message bus to said first module only if request for said message bus is not received from any modules in said second priority group, wherein said allocating allocates said message bus according to a least recently used (LRU) approach among modules in said first priority group if more than one module in said first priority groups requests said message bus.

[Claim 11] 11. A system comprising:

a message bus containing a plurality of signal lines including a first signal line and a second signal line;

a first module and a second module sharing said message bus to transfer data to each other; and

an arbitration module allocating said message bus to one of said first module and said second module,

wherein said first module requests access to transmit data on said message bus using said first signal line and transmits a bit of each of a plurality of packets to said second module on said first signal line,

said arbitration module indicating that said message bus is granted to said first module on said second signal line, wherein said first module transmits another bit of each of said plurality of packets on said second signal line to said second module.

[Claim 12] 12. The system of claim 11 , further comprising a plurality of modules including said first module and said second module, wherein each of said plurality of modules is assigned to one of a plurality of priority groups, said plurality of groups including a first priority group and a second

priority group, wherein said first module is assigned to said first priority group, said second priority group having a higher priority than said first priority group,

wherein said arbitration module allocates said message bus to modules in said first priority group only if a request is not received from any modules in said second priority group,

said arbitration module allocating said message bus to modules in said first priority group according to a least recently used (LRU) approach.

[Claim 13] 13. The system of claim 11 , further comprising a plurality of modules including said first module and said second module, wherein said message bus further comprises a BUSY line shared by each of said plurality of modules,

wherein said first module determines whether said BUSY line is asserted, wherein said BUSY line indicates whether any of said plurality of modules is transmitting on said message bus;

wherein said first module requests ownership of said message bus by sending a request on said first signal line if said BUSY line is not asserted.

[Claim 14] 14. The system of claim 13, wherein said first module asserts said BUSY line to indicate ownership of said message bus after said second signal line indicates that said message bus is granted to said first module.

[Claim 15] 15. The system of claim 13, wherein said first module sends a control packet on said message bus, wherein said control packet contains a first address representing an address of said second module and a number of packets to be transferred, wherein one bit of said control packet is sent on said first signal line and another bit of said control packet is sent on said second signal line.

[Claim 16] 16. The system of claim 15, wherein said second module receives said control packet and determines that said number of packets are directed to said second module by comparing said first address to a self address of said second module, said second module asserting a TRDY line to indicate that said second module is ready to receive said number of packets, wherein said first module sends said number of data packets on said message bus upon assertion of said TRDY line.

[Claim 17] 17. The system of claim 16, wherein said second module determines whether an uncorrectable error is present in a first packet, wherein said first packet is comprised in said number of data packets, said second module asserting a ERR signal line in said message bus to indicate

presence of said uncorrectable error, wherein said first module sends said first packet again upon said ERR signal line being asserted.

[Claim 18] 18. The system of claim 17, wherein said second module receives said first packet again and asserting said ERR signal line and a STOP signal if said uncorrectable error is detected again in said second module, wherein transferring said number of data packets is terminated by said first module upon assertion of said ERR signal line and said STOP signal.